

REMARKS

The Examiner's Office Action of January 5, 2005 has been received and its contents reviewed. Applicants would like to thank the Examiner for the consideration given to the above-identified application.

Claims 3-10, 16-33 and 35-42 are pending for consideration, of which claims 3, 4, 16, 18, and 35 are independent. In view of the following remarks, reconsideration of this application is now requested.

Referring now to the detailed Office Action, the specification stands objected to as lacking proper antecedent basis for the limitation "said gate wiring" recited in claims 3, 4, 16, 18 and 35. In response, Applicants respectfully direct the Examiner's attention to the Supplemental Amendment filed November 22, 2004 wherein claims 3, 4, 16, 18 and 35 were amended to further recite "a gate wiring electrically connected to said gate electrode". Support for this amendment may be found at least in, e.g., page 37, line 25 to page 38, line 2 of the specification.

Incidentally, Applicants note that a recent review of this application using PAIRS revealed that the Supplemental Amendment filed November 22, 2004 was entered. However, it appears that only the Remarks portion of the response was scanned, while the amended claims appear to be absent. Accordingly, Applicants have attached herewith a courtesy copy of the Supplemental Amendment filed November 22, 2004 and respectfully request the Examiner to rectify the omission of the claim amendments submitted with the Supplemental Amendment.

Claims 3, 4, 16, 18 and 35 stand rejected under 35 U.S.C. §112, second paragraph, as indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. The Examiner asserts that the limitation "wherein a first portion of said source wiring overlapped with said gate wiring has smaller line width than a second portion of said source wiring not overlapped with said gate electrode" is not understood and is assumed to read as "wherein a first portion of said source wiring overlapped with said gate wiring has smaller line width than a second portion of said source wiring not overlapped with said gate wiring". In response, Applicants note that the Supplemental Amendment filed November 22, 2004 further amended claims 3, 4, 16, 18 and 35 to provide a consistent usage of the words "gate wiring".

Claims 3-10, 16-25 and 27-33 stand rejected under 35 U.S.C. §103(a) as unpatentable over Matsumoto (U.S. Patent No. 5,323,042 – hereafter Matsumoto) in view of Ikeda (JP 7-326767 – hereafter Ikeda), Otani (JP 10-56184 – hereafter Otani) and Toyoda (JP 5-61069 – hereafter Toyoda). Further, claims 4 and 23 stand rejected under 35 U.S.C. §103(a) as unpatentable over Yeo (U.S. Patent No. 6,140,162 – hereafter Yeo) in view of Ikeda, Otani and Toyoda. These rejections are respectfully traversed at least for the reasons provided below.

Applicants note that the above-summarized rejections appear to be similar to the rejections in the Office Action mailed July 13, 2004 except for the difference where the Toyoda reference is cited in place of the previously applied Okabe reference (JP 63-222443).

In the rejections, the Examiner alleged that “Toyoda discloses in Fig. 1 a display device comprising a first portion 8 of a source wiring 5 overlapped with said gate wiring 3 having a smaller line width than a second portion of said source wiring not overlapped with said gate wiring, and a portion of said second portion overlaps with a pixel electrode.” However, Applicants are unable to find such a disclosure in Toyoda. Rather, according to Fig. 1 of Toyoda, the source wiring 5 does not overlap with the pixel electrode 2. Hence, the Examiner’s allegation appears to be insupportable. Should the Examiner still maintain the rejection based on the alleged teaching of Toyoda to cure the deficiencies of Matsumoto, Ikeda and Ohtani, Applicants would respectfully request the Examiner to point out the specific text in Toyoda supporting the Examiner’s allegation.

The requirements for establishing a *prima facie* case of obviousness, as detailed in MPEP § 2143 - 2143.03 (pages 2100-122 - 2100-136), are: first, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference to combine the teachings; second, there must be a reasonable expectation of success; and, finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations.

Applicants respectfully assert that the cited prior art references fail to teach, disclose or suggest at least the features wherein a pixel electrode over said source wiring and a first portion of said source wiring overlapped with said gate wiring has smaller line width than a second portion of said source wiring not overlapped with said gate wiring, and a portion of said second portion overlaps with said pixel electrode as recited independent claims 3, 4, 16,

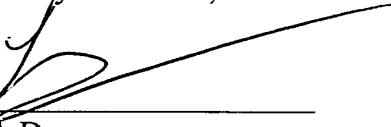
18 and 35 and their respective dependent claims. Hence, Applicants' claimed invention is distinguishable over the cited prior art references.

In the interest of keeping prosecution history compact, and the arguments set forth above with respect to Toyoda are deemed sufficient to overcome the pending rejections, Applicants will not address each and every §103(a) rejection. Applicants reserve the right to do so in the future, as necessary.

In view of the arguments set forth above, the Applicants respectfully request reconsideration and withdrawal of all the pending rejections.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise, which could be eliminated through discussions with Applicants' representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby be expedited.

Respectfully submitted,



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